Optical Phase Locked Loop

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This lab note describes an optical phase-locked loop (OPLL) that uses digital phase frequency detector (PFD) circuits. The OPLL is shown in Figure 1 and is used to beatnote lock a DBR diode laser to a fiber laser from NKT. The system is housed in a rack box as shown in Figure 4. The box previously included an optical frequency doubler in order to generate green light for locking the system to a wavelength meter.

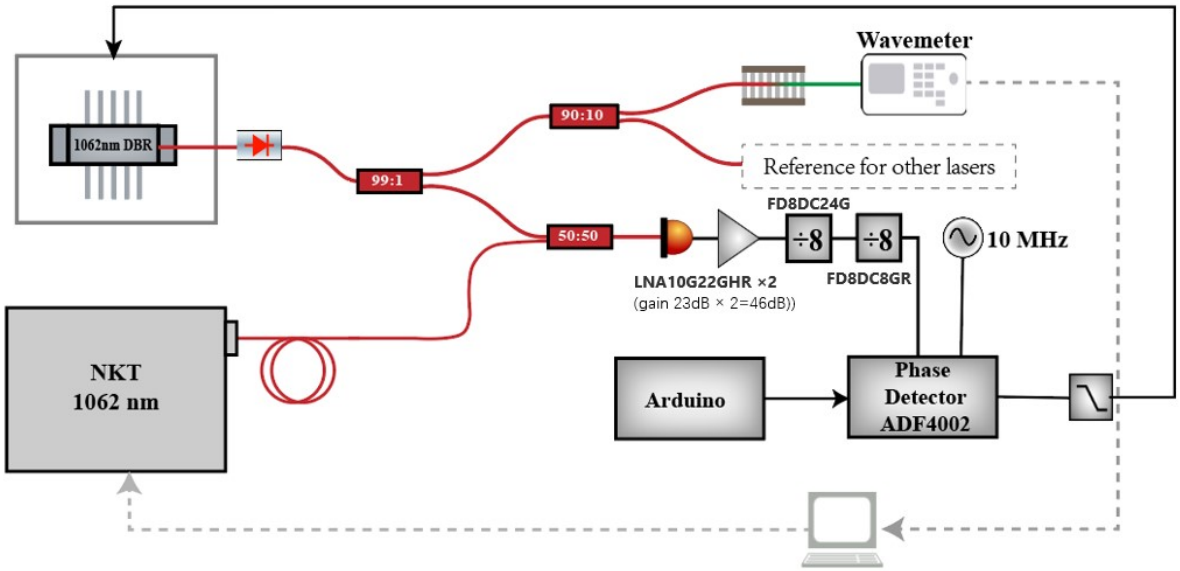

Figure 1: Schematic of the OPLL

1 Optimization of OPLL Settings

OPLLs operates on the same principle as a standard Phase Locked Loop (PLL) used in electronics. The only difference is that in OPLL the beatnote signal of two lasers replaces the Voltage Controlled Oscilator (VCO) in a standard PLL.

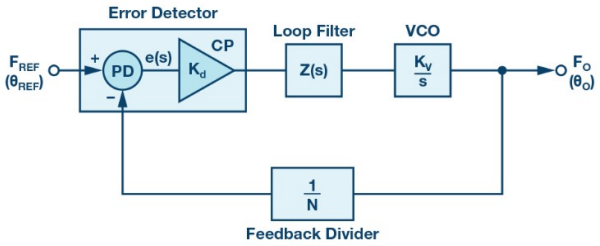

Figure 2: Basic PLL configuration (from Analog Devices PLL Fundamentals)

Optimizing the control parameters of an OPLL is necessary to achieve better performance. Faster lock time (the time needed for the system settle to a new set point) and better suppression of laser phase noise are desired, which can be achieved with a larger loop bandwidth. However, self-oscillation must be

avoided. Empirically, the bandwidth of the loop filter should be equal to or less than 1/10 of the PFD frequency to prevent self-oscillation.

In our setup, the performance of the OPLL is optimized for an 16 GHz laser frequency offset by adjusting the loop filter and the parameters in the ADF4002 phase frequency detector.

The laser frequency offset follows this relationship when the OPLL is working.

$$laser\ frequency\ offset = reference\ frequency/R\ Counter \times N\ Counter \times frequency\ dividing\ factor$$

The OPLL uses the 10 MHz GPS Clock as the reference. As shown in Figure1, there are two 8-frequency dividers in the loop, and the total frequency dividing factor is 64. For a higher PFD frequency, the R counter is set to be 1, so that $PFD\ frequency = reference\ frequency/R\ Counter = 10\,\text{MHz}$. Control of the PFD ADF4002 is accomplished via an arduino DUE using SPI, and the arduino code *ADF4002_OPLL.ino* is provided.

Table 1: PFD settings

Charge Pump Current	5mA
N counter	25
R counter	1

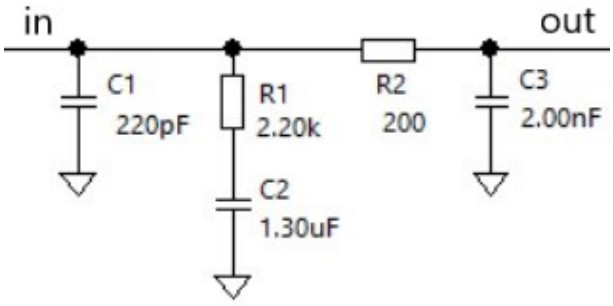

Figure 3: loop filter parameters

Shown in Figure 3 is the design of the loop filter. A fast lock time * is achieved under the given parameters. The bandwidth of the loop filter is $\sim$ 150kHz. When adjusting the loop filter components, it is important to exercise caution as the PCB board is fragile.

Following the output of the loop filter, a voltage follower circuit is soldered onto the ADF4002 evaluation board. The signal voltage is then attenuated by a 6dB attenuator and connected to the DC modulation port of the Koheron diode driver CTL200. The modulation gain of CTL200 is set to the "M setting".

With the optimized settings, the OPLL achieves a lock time of approximately 10μs. The system has a capture range of $\sim$1.6GHz, which is sufficient for locking the DBR automatically since the DBR laser will never drift thus far.

This OPLL does not demonstrate good phase noise suppression performance for the DBR laser. Although the phase noise of the 64-divided beatnote signal is fairly low, the phase noise before dividing at 16 GHz is not significantly suppressed. This is due to the frequency divider's effect on phase noise conversion. Dividing a signal frequency by N reduces the phase noise of the output signal by 20log (N) dB. The loop does not have enough gain at high frequency for phase noise suppression because of excessive division. To improve performance, using fewer dividers and a PLL chip with a higher PFD frequency is recommended. †

*The lock time is measured using the following method. We use a frequency modulated (FSK) signal as the reference.The PFD output signal is observed using an oscilloscope, and the time required for the PFD output signal to settle to a new value after a rapid change in the reference frequency is recorded as the settle time.

†In order to explore better phase noise suppression performance, one of the 8 dividers was removed from the original scheme,

2 the OPLL Rack Box

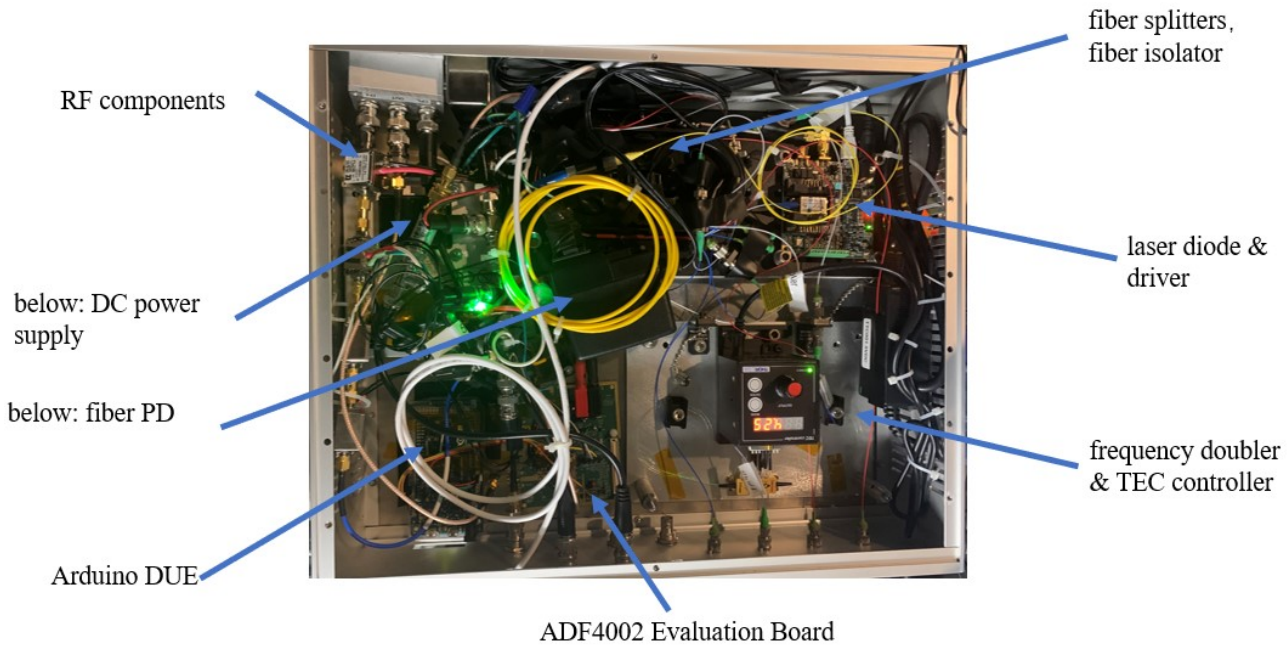

Figure 4: top view of the box

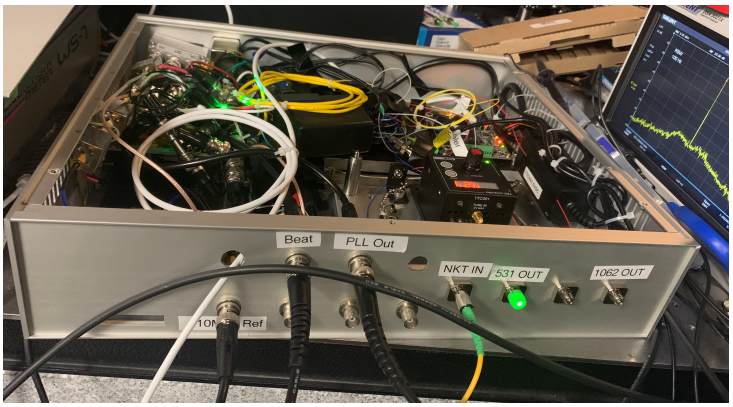

Figure 5: front view of the box

The OPLL system is contained within a rack box that houses the diode laser, fiber optical components, a fast fiber photo detector (PD), RF components, a PLL evaluation board, and their respective power supplies. The front panel of the box features BNC connectors for RF reference input and PLL monitoring. Fiber connectors are also available for inputting the reference laser and outputting the offset locked light and frequency doubled light.

3 Schematic of an OPLL for Frequency Chirping and Frequency Jumping

The large capture range of the OPLL based on digital PFD enables frequency chirping and frequency jumping, which allows for the use of a single laser for multiple purposes.

and the offset was set around 2GHz. This modification resulted in a significant improvement, with a 30 dB phase noise suppression demonstrated, surpassing the performance of the original scheme.

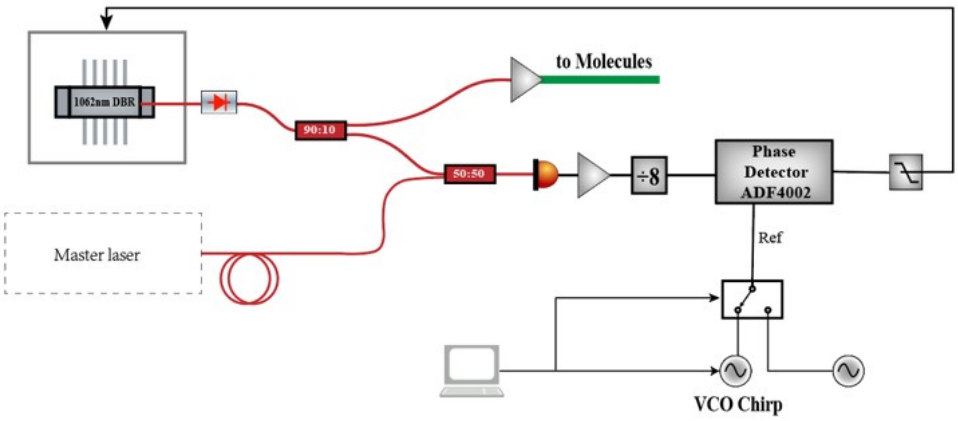

Figure 6: an OPLL for frequency chirping and jumping